PRESENTACIÓN

KDT JU

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KDT Programme Officer

KDT JU

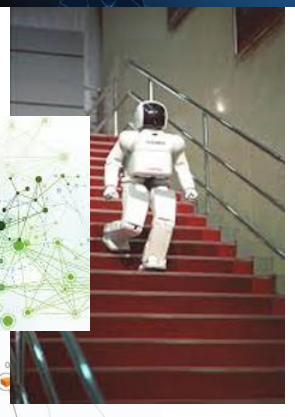
KEY DIGITAL TECHNOLOGIES JOINT UNDERTAKING

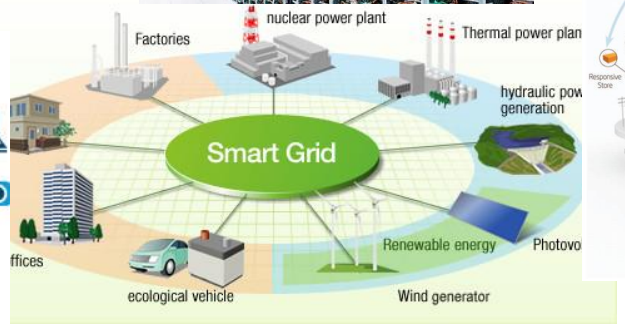
EUROPEAN PARTNERSHIP

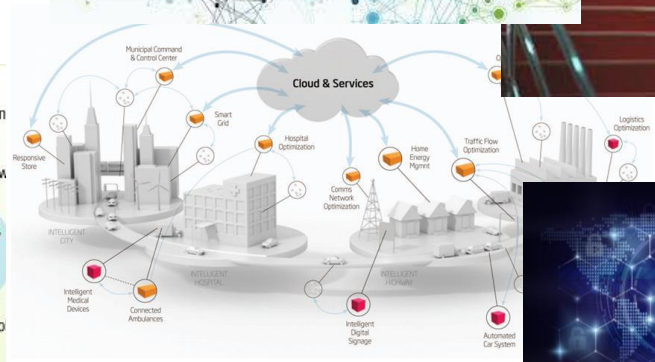
OUTLINE

- Introduction KDT JU
- Towards CHIPS JU
- Chips for Europe Initiative
- Activities in Chips JU:
  - Design Platforms
  - Pilot lines
  - Competence Centres/Skills

KDT PREPARES FOR THE FUTURE







FROM ENIAC/ARTEMIS TO KDT JU

First generation JUs ENIAC & ARTEMIS JU 2008-2014

- full bottom-up
- 2011-2013**: pilot lines, building critical mass**
- payments of EU funding part linked to national cost recognition
- start as first of its kind **tripartite** in the universe of European institutions

Second generation JU ECSEL JU 2014-2021

- along the **value chain**
- focussed on **industrial leadership** that promote **synergies** between commercial strategies and societal needs
- full bottom-up **with some special topics** that re-inforce/align national strategies and European priorities
- programme based on the **common agenda of** Europe's ECS
- **lighthouse initiatives**: Mobile.E, Industry4.E, Health.E
- payments of EU funding based on H2020 rules, national funding on national cost recognition (with few NA adopting the H2020 rules)
- start as merger of the first two joint undertakings: growing bigger

KDT JU GOVERNANCE

Union Body with Legal Personality

Governing Board
ECSEL Members
(Public Authorities, Private Members)

- **Strategic orientation, supervision**

Approves MultiAnnual Strategic Plan (MASP), Work Plan (WP), rules, membership, budget, staff, policies

Executive Director
Programme Office

- **Chief Executive, legal representation**

Consolidates MultiAnnual Strategic Plan MASP, elaborates budget proposal, Work Plan WP, executes calls; monitors projects

Public Authorities Board
European Commission,
ECSEL Participating States

- **Representatives of the Public Authorities**

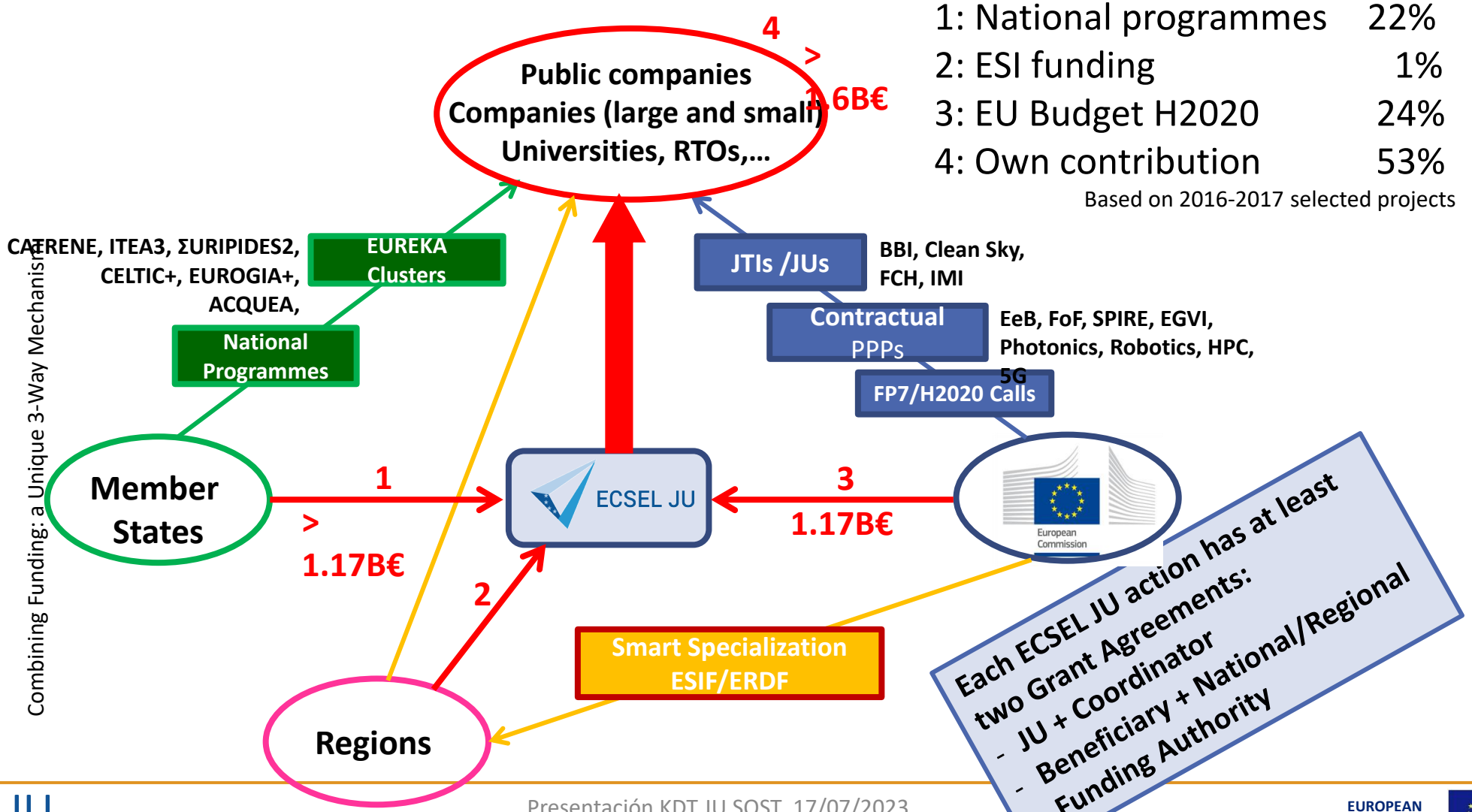
Approves call launching, call rules, allocates funding

Private Members Board
AENEAS, ARTEMIS-IA, EPoSS

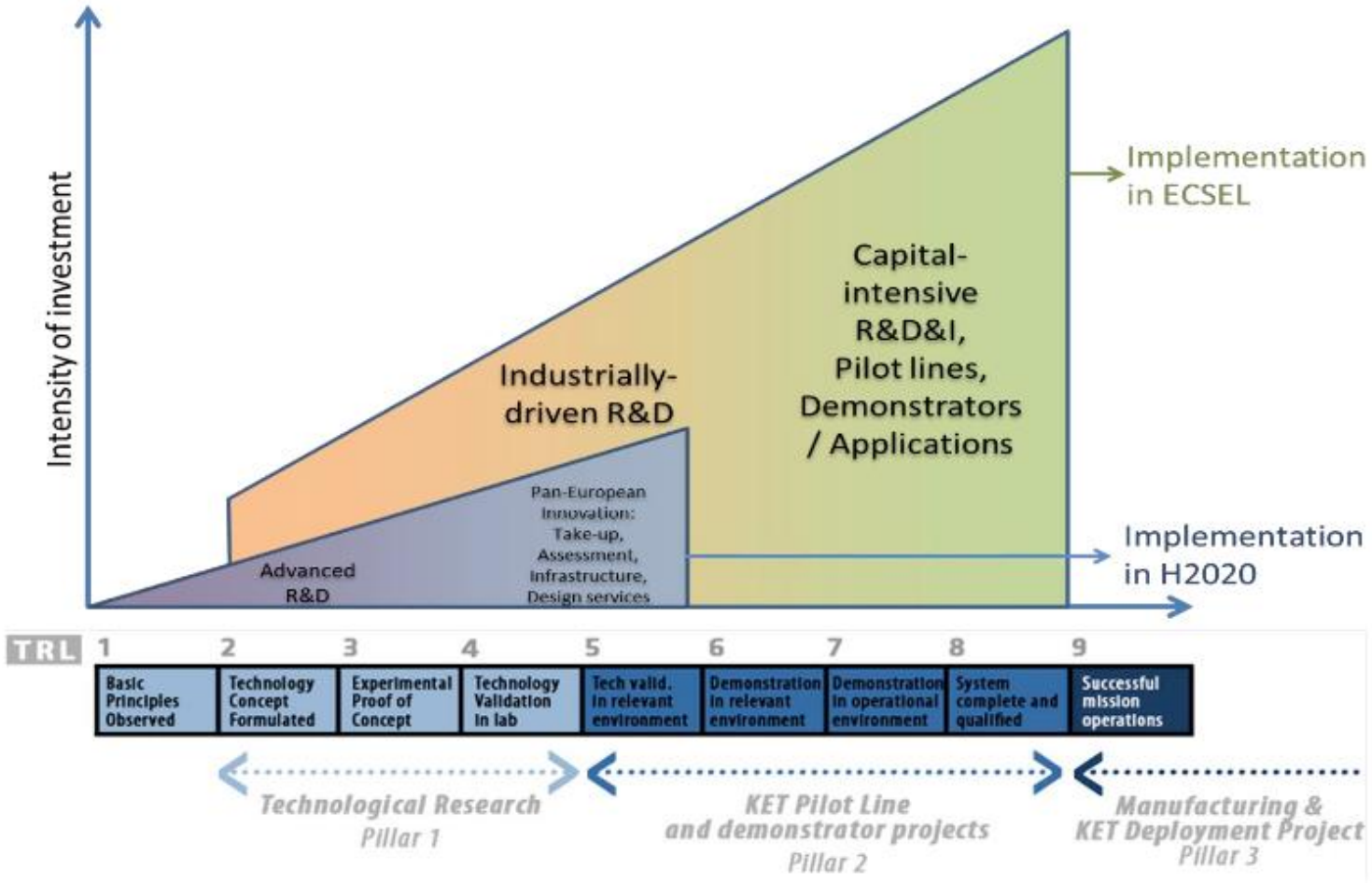
- **Defines research agenda**

Elaborates the multiannual strategic research and innovation agenda (MASRIA) and the annual research and innovation activities plan (RIAP)

ECSEL JU MECHANISM

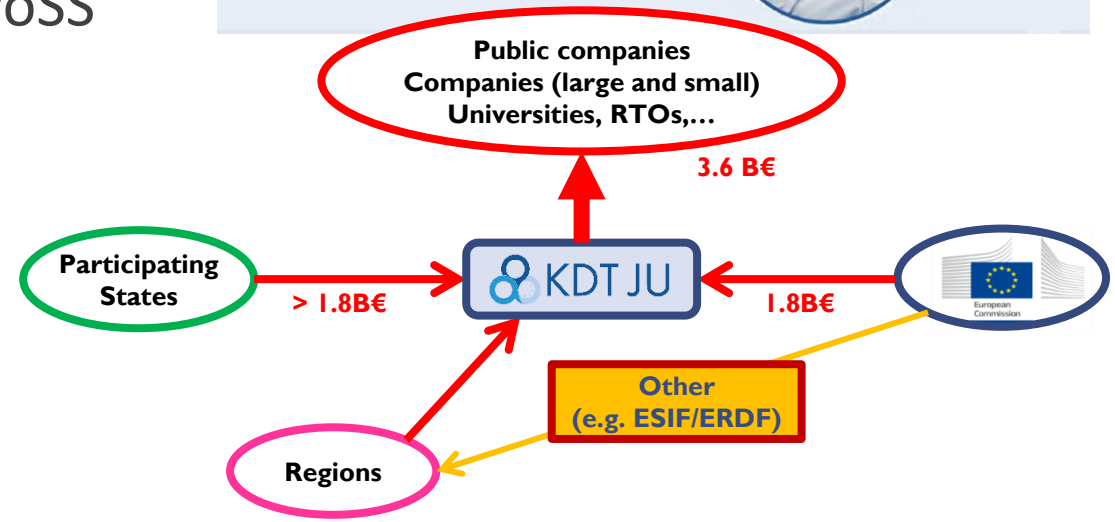


H2020 vs ECSEL JU



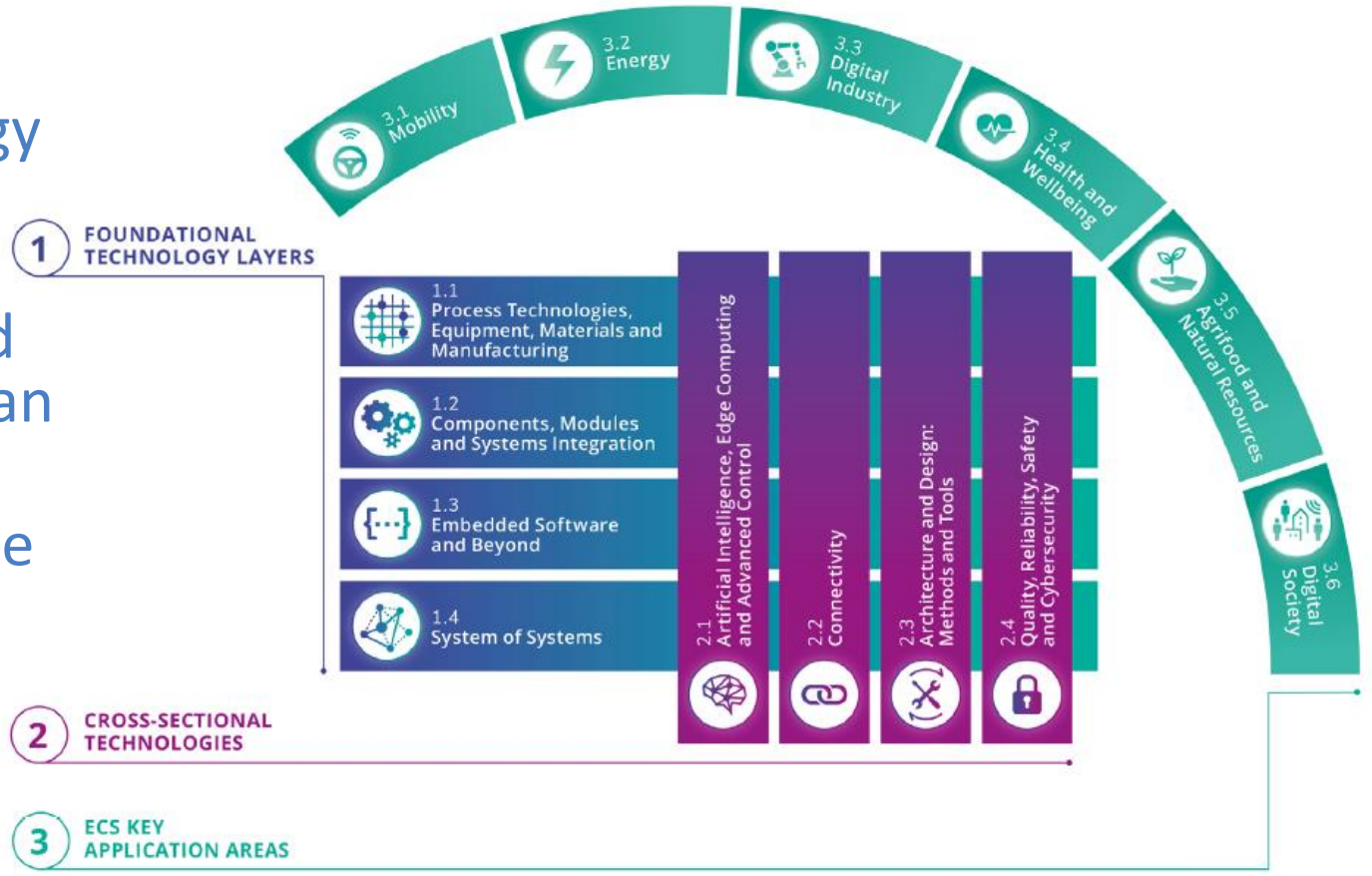
KDT JU 2021-2027

- KDT JU = Key Digital Technology Joint Undertaking
- 3rd generation
- Tripartite
  - European Commission
  - Participating states (29)
  - Industry associations = AENEAS, INSIDE, EPoSS
- Started : 30 November 2021 (ECSEL JU ➲ KDT JU)
- Budget ambition : 6B€ funded by 1,8 B€ (EU) + 1,8 B€ (national)
- Regulation under Horizon Europe



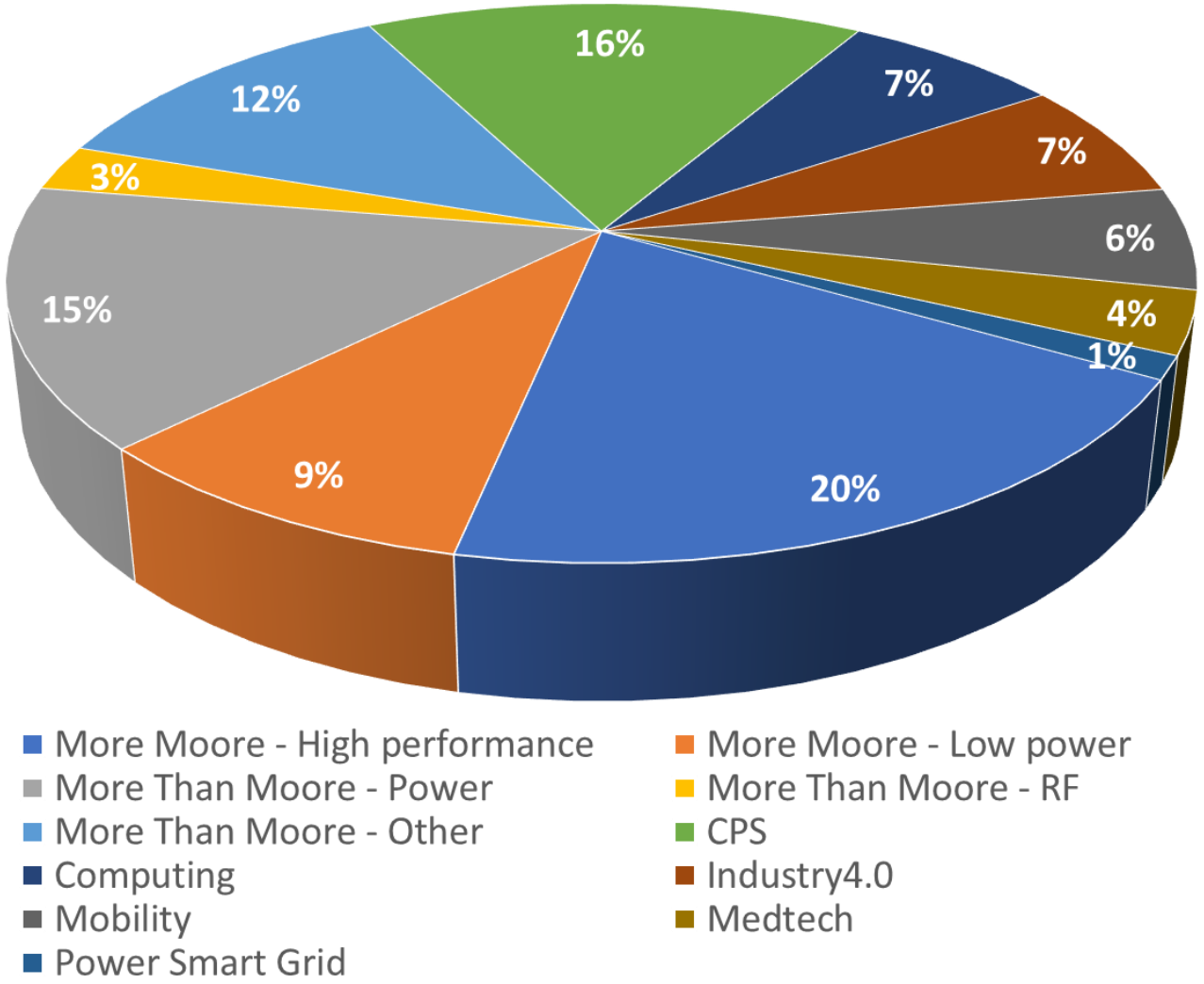
ECS SRIA

- Boost **industrial competitiveness** through **interdisciplinary** technology innovations
- Ensure/reinforce **EU strategic autonomy** through secure, safe and reliable ECS supporting key European application domains
- Establish and strengthen sustainable and resilient ECS value chains supporting the **Green Deal**
- Unleash the full potential of intelligent and autonomous ECS-based systems for the **European digital era**



PROJECT PORTFOLIO (2014-2021)

- 111 projects including 5 CSAs
- 3 775 beneficiaries
- 5 430 M€ of costs
- 2 600 M€ in funding (EU + national)
- 470 500 Persons-month
- Project participants from all participating states



KDT 2023 – LAST CALL

- IA
  - Open call
  - 6G Integrated Radio Front-End for TeraHertz Communications
  - Integration of trustworthy Edge AI technologies in complex heterogeneous components and systems
  - Electronic Control Systems (ECS) for management & control of decentralized energy supply & storage
  - Improving the global demand supply forecast of the semiconductor supply chain
- RIA
  - Open call
  - Hardware abstraction layer for a European Vehicle Operating System
- CSA
  - Pan-European network for Advanced Packaging made in Europe
  - Coordination of the European software-defined vehicle platform
- Timeline: open on 7 February 2023; Project outline phase closing on 3 May 2023

STRUCTURE, TOPICS, EU BUDGET

Action	Topic	Estimated EU Expenditure (M€)
Call 2023-1-IA T1	Global call according to SRIA 2023	153.0
Call 2023-1-IA T2	Focus topic 6G Integrated Radio Front-End for TeraHertz Communications	20.0
Call 2023-1-IA T3	Focus topic on Integration of trustworthy Edge AI technologies in complex heterogeneous components and systems	20.0
Call 2023-1-IA T4	Focus Topic on Electronic Control Systems (ECS) for management & control of decentralized energy supply & storage	20.0
Call 2023-2-RIA T1	Global call according to SRIA 2023	76.7
Call 2023-2-RIA T2	Focus Topic on Hardware abstraction layer for a European Vehicle Operating System	20.0
Call 2023-3-IA T1	Improving the global demand supply forecast of the semiconductor supply chain	5.0
Call 2023-3-CSA T2	Pan-European network for Advanced Packaging made in Europe	1.0
Call 2023-3-CSA T3	Coordination of the European software-defined vehicle platform	2.0
	Total	**317.7 M€**

NATIONAL BUDGETS

National funding shall be commensurate to the EU funding rates

Participating states	2023-1 T1	2023-1 T2	2023-1 T3	2023-1 T4	2023-2 T1	2023-2 T2	Total
AT	3.7	0	0.5	0	1.6	1.2	7.0
BE-FL							12.0
BE-BR							1.0
BE-WL							0.4
CY							3.0
CZ	1.1	0.2	0.2	0.2	1.1	0.2	3.0
DE		0.0					32.0
EE							0.75
EL							0
ES AEI							3.0
ES MAETD							5.0
FI							10.0
FR							30.0

Participating states	2023-1 T1	2023-1 T2	2023-1 T3	2023-1 T4	2023-2 T1	2023-2 T2	Total
HU							2.0
IE							2.0
IL							3.5
IT MIMIT							20.0
IT MUR							14.0
NL							30.0
NO							0.0
PL							1.5
PT							1.5
SE	1.9	0.4	0.2	0.0	1.9	0.0	4.4
SK							0.8
TR							6.0
Total							192.85

For DE: Total 16.0 for IA Calls T1, T3 and T4 plus total 16.0 for RIA Calls

EVOLUTION UNDER KDT JU TOWARDS CHIPS JU

BOTTOM UP VERSUS TOP DOWN - EU VERSUS NATIONAL SYNERGIES

FOCUS TOPICS

Special topics, special calls, nudges, % of budget, special criteria (national), …

Selection taking into account national synergies

SRIA as basis for WP, consortia building, support by associations, topic selection

Proposals submitted by the community in regular calls for all open topics

GB, WP @ or before launch

PAB @ selection

Portfolio of projects

COOPERATION ASPECTS AKA SYNERGIES

Potential for synergies through cooperative actions

- **Smart Networks & Services**: initiative on 5G and 6G connectivity
- **European High Performance Computing**: initiative on underlying supercomputing capacities
- **Photonics, AI-Data-Robotics, Global competitive space system and Made in Europe**: synergies are needed where EU industry has to develop leadership and competitiveness in the global digital economy
- **Digital Europe Programmes** with testing facilities, skills development and capacity building activities in specific digital domains, similar for Connecting Europe Programmes
- **Health, Mobility and Energy** partnerships
- **IPCEI**, other national programmes
- **Eureka** clusters
- Coordination with **regional clusters** such as Silicon Europe, Silicon Saxony (Dresden), Minalogic (Grenoble), and DSP Valley (Leuven-Eindhoven)

European Partnerships

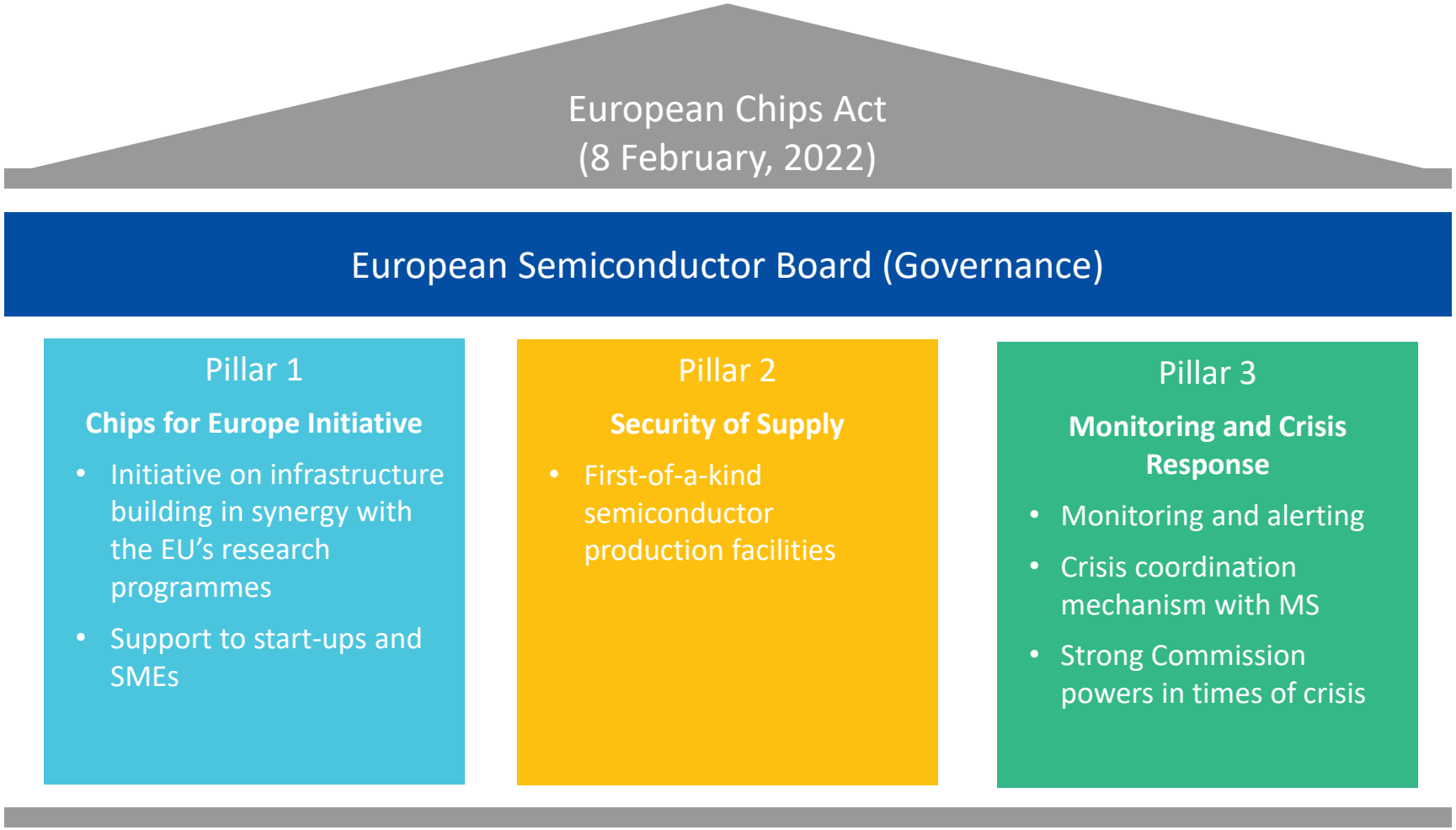
HORIZON EUROPE PILLAR II - Global challenges & European industrial competitiveness

CLUSTER 1: Health	CLUSTER 4: Digital, Industry & Space	CLUSTER 5: Climate, Energy & Mobility	CLUSTER 6: Food, Bioeconomy, Agriculture, …
Innovative Health Initiative	Key Digital Technologies	Clean Hydrogen	Circular Bio-based Europe
Global Health Partnership	Smart Networks & Services	Clean Aviation	Rescuing Biodiversity to Safeguard Life on Earth
Transformation of health systems	High Performance Computing	Single European Sky ATM Research 3	Climate Neutral, Sustainable & Productive Blue Economy
Chemicals risk assessment	European Metrology (Art. 185)	Europe's Rail	Water4All
ERA for Health	AI-Data-Robotics	Connected and Automated Mobility (CCAM)	Animal Health & Welfare*
Rare diseases*	Photonics	Batteries	Accelerating Farming Systems Transitions*
One-Health Anti Microbial Resistance*	Made in Europe	Zero-emission waterborne transport	Agriculture of Data*
Personalised Medicine*	Clean steel – low-carbon steelmaking	Zero-emission road transport	Safe & Sustainable Food System*
Pandemic Preparedness* *Co-funded or co-programmed*	Processes4Planet	Built4People	
	Global competitive space systems**	Clean Energy Transition	
		Driving Urban Transitions	

Institutionalised Partnerships (Art 185/7)
Institutionalised Partnerships / EIT KICs
Co-Programmed
Co-Funded

* *Calls with opening dates in 2023-24*
** *Calls with opening dates not before 2022*

The Three Pillars of the Chips Act



CHIPS FOR EUROPE INITIATIVE

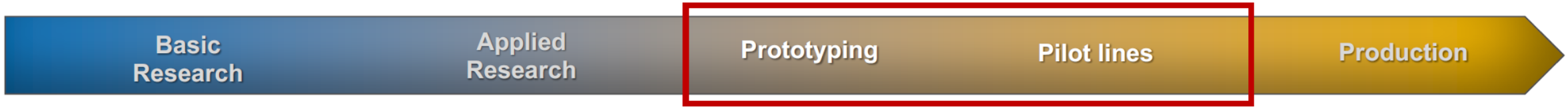
Bringing the gap from lab to fab

5 Objectives

1. Reinforce design capacity by providing a **virtual design platform**
2. Enhance existing and developing new **pilot lines**
3. Accelerate the development of **quantum chips**
4. Expand **skills** and set up a network of **competence centres**
5. Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

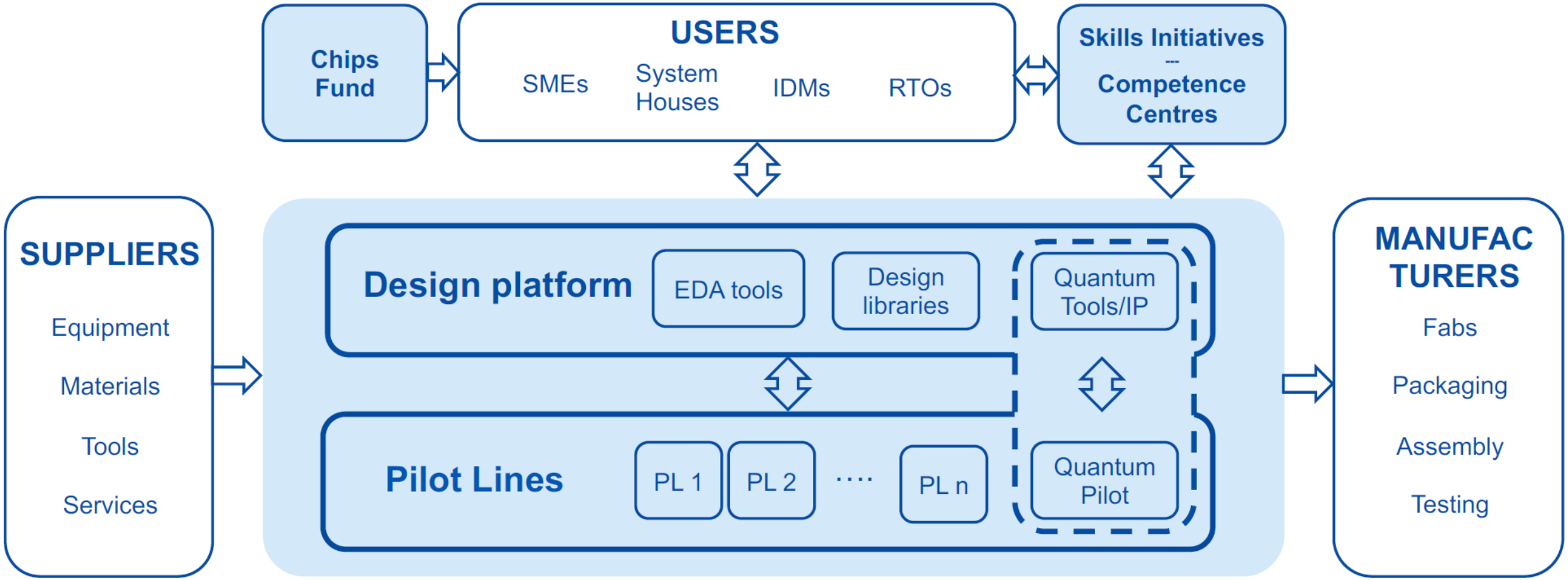
EIC
I-EU



European Commission

CHIPS FOR EUROPE INITIATIVE

Bringing the gap from lab to fab



DESIGN PLATFORMS

Scope

Ambition

Foster the development of the semiconductor **design ecosystem** in EU, reinforcing capacity to innovate and create European Intellectual Property through IC design

Main scope

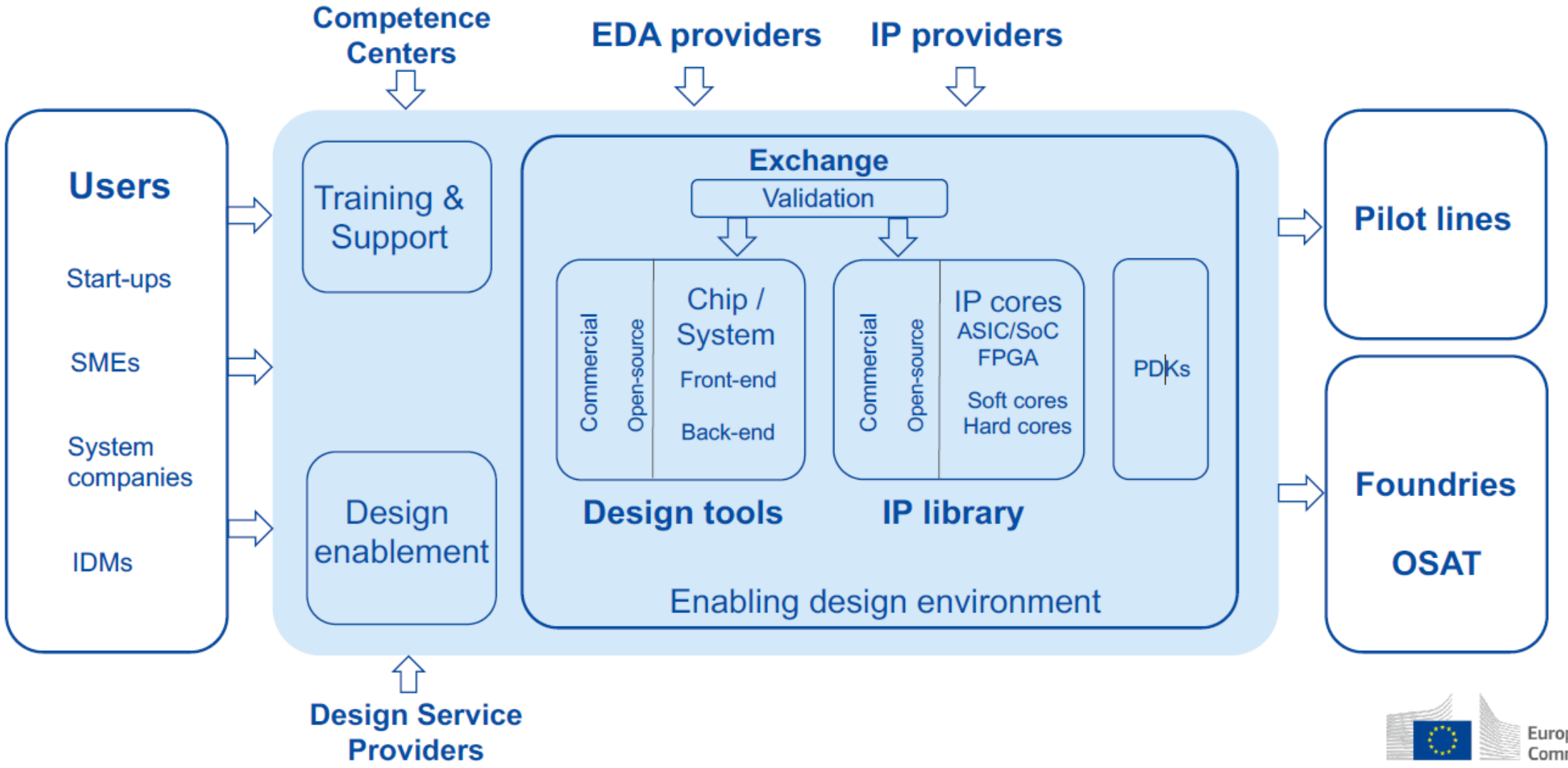
- **Reduce entry barriers** and admin burden for EU companies engaging in chip design
- **Facilitate access** to pilot lines and manufacturing facilities
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centers** offering **training** and support to boost design skills

Instrument

Develop a **virtual design platform,** offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

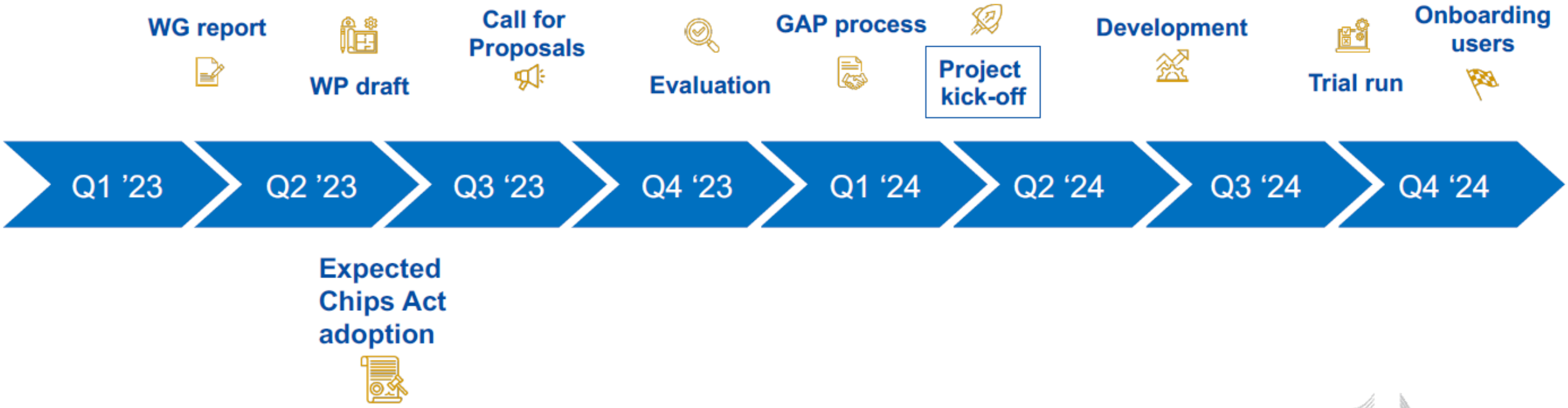
European Commission

DESIGN PLATFORMS



DESIGN PLATFORMS

Draft planning

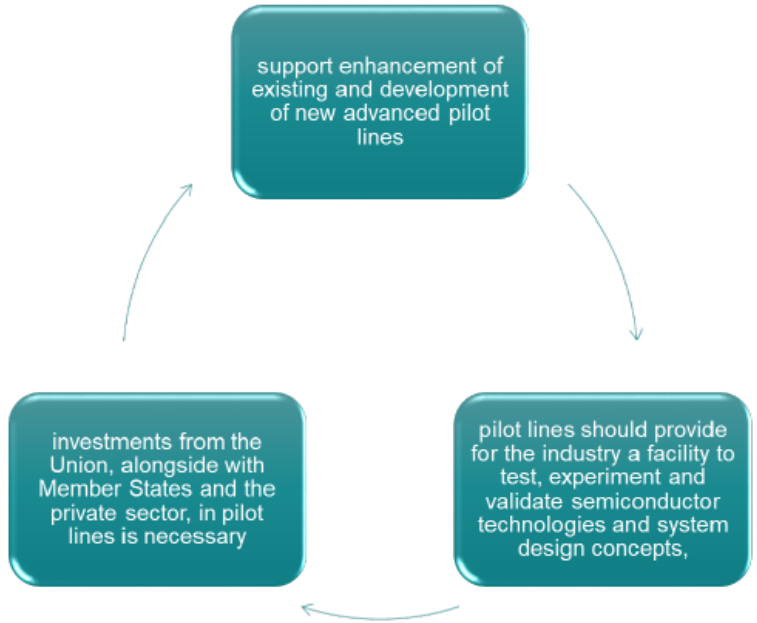


** Based on current estimation of the legislative process*

European Commission

PILOT LINES

General Approach

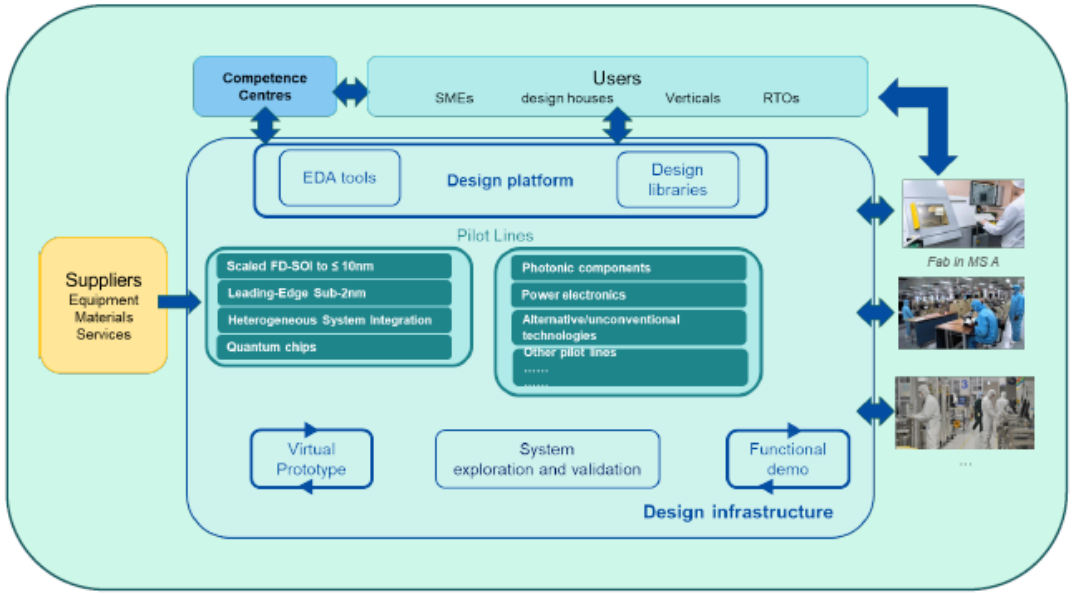


Operational objectives of the Chips for Europe Initiative:

ii) to provide the basis for strengthening the security of supply and the semiconductor ecosystem in the Union, the Initiative should **support enhancement of existing and development of new advanced pilot lines** to enable development and deployment of cutting-edge and next generation semiconductor technologies. **The pilot lines should provide for the industry a facility to test, experiment and validate semiconductor technologies and system design concepts**, while reducing environmental impacts as much as possible. **Investments from the Union, alongside with Member States and the private sector, in pilot lines is necessary** to address the existing structural challenge and market failure where such facilities are not available in the Union hindering innovation potential and global competitiveness of the Union

PILOT LINES

Goals



To establish a Pilot Line Infrastructure consisting of

- a set of new pilot lines that will play a central role, such as
  - *Scaled FD-SOI down to 10nm and below*
  - *Leading-edge process technology at 2nm and below*
  - *Advanced Heterogeneous System Integration*
- a set of new and existing pilot lines that will be established or upgraded to integrate complementary competences
- a link with the design platform as well as the whole ecosystem, including competence centres

PILOT LINES

Timeline implementation

Phases

1. Invitation to pilot lines hosting organisations *(2Q2023)*
2. Call for proposals *(3Q2023)*
3. Launch of first batch *(1Q2024)*

Other considerations

Participants, implementation, financing,…

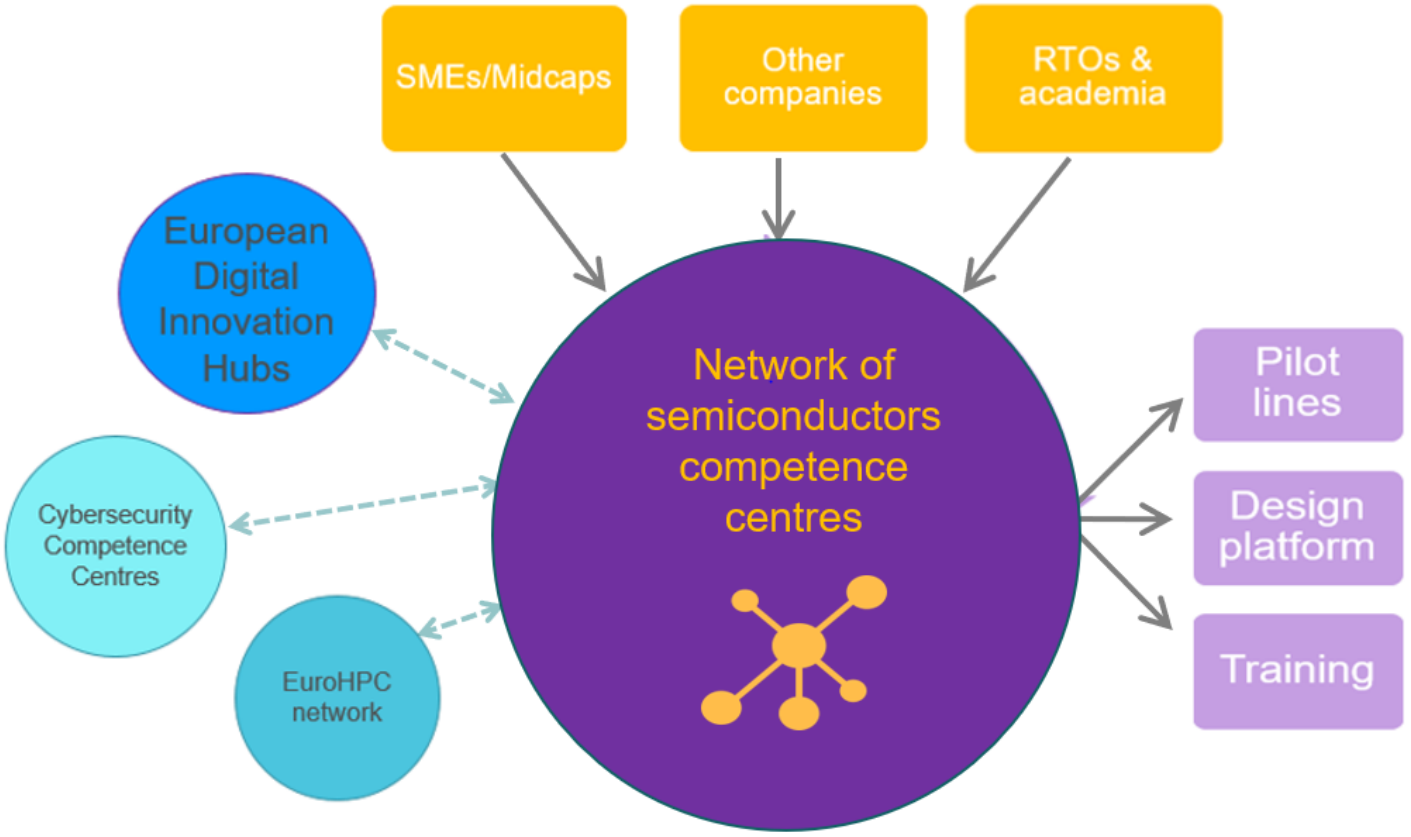
** Based on current estimation of the legislative process*

COMPETENCE CENTRES

- General Approach: "**Member States shall designate candidate competence centres** in accordance with their national procedures, administrative and institutional structures through an open and competitive process"
- **Chips JU Work Programme to set procedure** for establishing competence centres, including selection criteria, and further tasks and functions of centres
- **Chips JU to decide on selection** of competence centres
- Competence Centres to be set up via **restricted calls**, following candidate nominations by Member States (plus Iceland and Norway)
- Each Centre to be **funded on a 50-50 basis** by host country and Union

COMPETENCE CENTRES

Role of competence centres among stakeholders

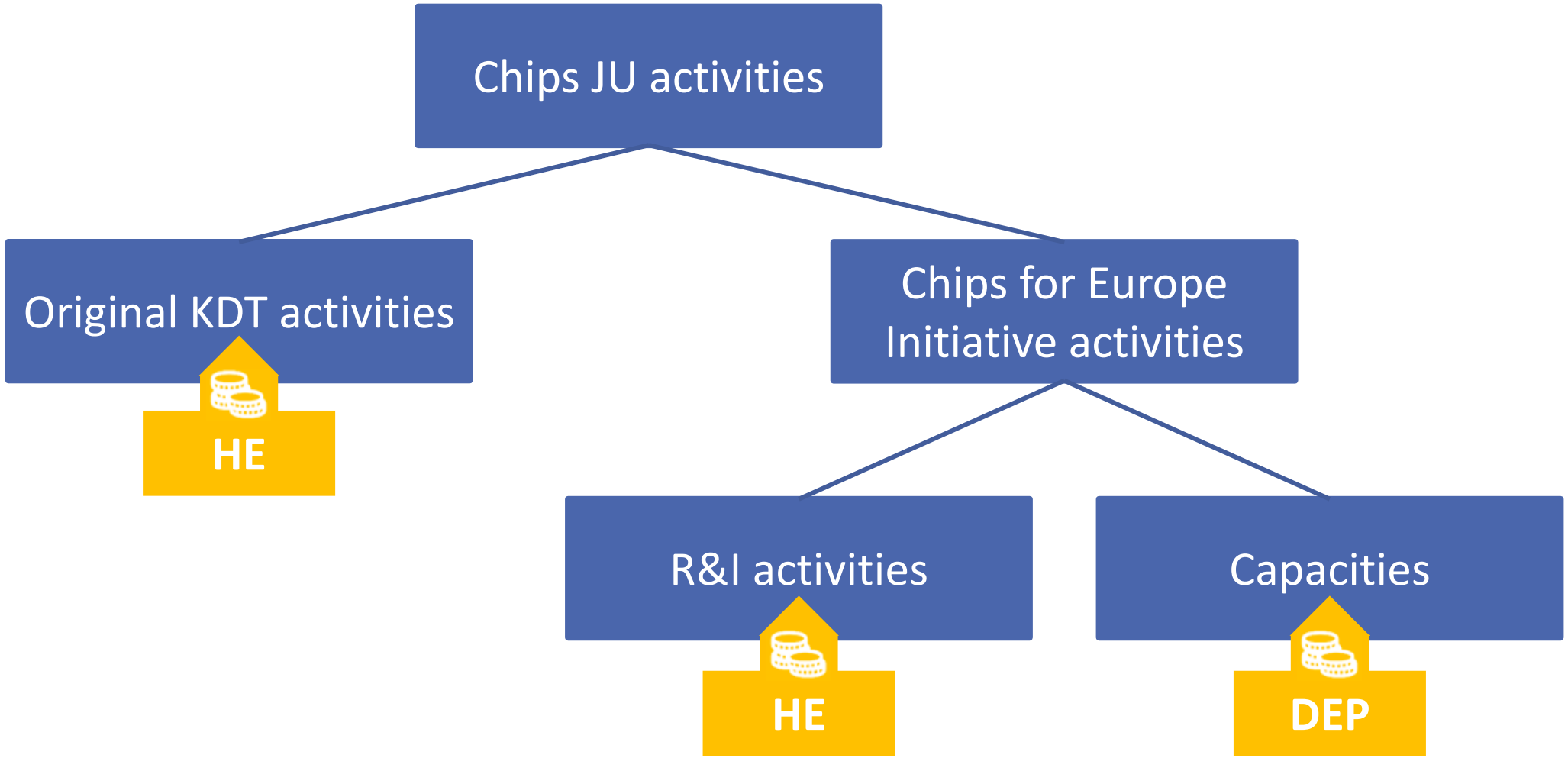


European Commission

COMPETENCE CENTRES

Date	Milestone
November 2022	Workshop with EDIHs, CCs, users, MS (Poland)
February 2023	Workshop with Competence Centre users
February 2023	First draft guidance document
March 2023	Discussion with MS on implementation (PAB meeting)
April 2023	Consultation with stakeholders + MS
May 2023	Final version of guidance document
September 2023	Call for proposals launch
February 2024	Selection of proposals by PAB
May 24	Launch of first batch of competence centres

ENVISIONED BUDGET AND ACTIVITIES STRUCTURE IN CHIPS JU



ENLACES DE INTERÉS

- Council of the EU:

  https://www.consilium.europa.eu/en/press/press-releases/2022/12/01/chips-act-council-adopts-position/

- European Commission. European Chips Act:

  https://digital-strategy.ec.europa.eu/en/policies/european-chips-act

- AENEAS:

  https://aeneas-office.org/2022/05/23/ec-staff-working-document-on-eu-chips-act/

- European Commission. Staff Working document:

  https://digital-strategy.ec.europa.eu/en/library/european-chips-act-staff-working-document

- KDT JU:

  https://www.kdt-ju.europa.eu/

Gracias por su atención

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